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Design of a Modified Carry Select Adder with Single Fault Tolerant Architecture

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Abstract: In the era of deep sub-micron technology, probability of chip failure has been increased with increase in chip density. A system must be fault tolerant to decrease the failure rate and increase the reliability of it. The major bases of VLSI areas are low power, high speed and data logic design. Adder forms the integral part of ALU. Different algorithm in digital signal processing such as FIR and IIR are also employed using adder. Advance result can be calculated by using possible values of input carry 0 and 1. Here carry select adder is modified with BEC and Brent kung adder. In addition triple fault tolerant architecture is implemented in the modified carry select adder. Multiple faults can affect a system simultaneously and there is a trade of between area overhead and number of faults tolerated. The proposed system models fault tolerant architecture design for modified carry select adder and a conditional sum adder as fast adder assuming single double and triple faults.

Keywords: ALU, BEC, BK.

I. INTRODUCTION

Adder is absolutely essential block in computer and other digital devices. It not performs addition of any given of numbers but it is also utilized to calculate the addresses or the operational codes. A fault tolerant design enables a system to continue its intended operation, possibly at a reduced level rather than failing completely when some part of the system fails.

A. Fault tolerant architecture in adder

Fault tolerant is the property that enables a system to continue operating property in the event of the failure of some of its components. Fault tolerant design enables a system to continue its intended operation possibly at a reduced level rather than failing completely when some part of the system fails. The term is most commonly used to describe computer systems designed to continue more or less fully operational with, perhaps a reduction in throughput or an increase in response in the event of some partial failure. A structure is able to retain its integrity in the presence of damage due to causes such as fatique, corrosion, manufacturing flaws, or impact. Within the scope of an individual system, fault tolerance can be achieved by anticipating exceptional conditions and building the system to cope with them, and in general aiming for self-stabilization so that the system converges towards an error free state. Fault tolerant can be defined as the ability to continue operating after the failure of a given system component. To be fault tolerant a system must have one or more redundant components that can take over the function when the primary component fails. In addition, the system must have both a means of detecting failures in the components and a means of transferring to working components after a failure has been detected .Fault tolerant system configurations are used extensively in processes where the system must remain on line in the event of component failure. Adder is absolutely essential block in any digital architecture. Among different types of adders carry select adder is most popular because of its less delay and required modifications can be made in the carry select adder. It has also high throughput for bit level pipelining. Fault tolerant designs are also cascaded to increase the number of input bits making a system module wise self-reconfigurable is more cost effective and hardware efficient rather than trying to make the whole system fault tolerant at a time. Carry select adder is the fastest adders used in many computer data processing processors to perform the fast arithmetic functions. This work used a simplest and efficient transistor level modification in BEC-1 converter to significantly efficient the power and area of the carry select adder. In modified carry select adder eliminates all the redundant logical operations used in the regular carry select adder and proposed a new logic formulation for carry select adder. The carry select operation is scheduled before the theoretical calculation of final sum, which is different from the conventional approach value. Bit patterns of two anticipating carry words and fixed bits cin are used for logical techniques of carry select and generated units. A better carry select adder design is obtained using logic units.

B. Carry select adder with BEC

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. A regular CSLA circuit uses two RCAs through which the sum and carry outputs are generated. One of the RCA block propagates a carry 0 and the other RCA block propagates carry 1. Multiplexers are provided at

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each RCA block to select the carry output. This selection of carry outputs increases the speed of operation of the adder but require more area as it uses two RCAs and as a result it consumes more power. In order to reduce the area and power consumption a modified CSLA is proposed. The modified CSLA proposed here is a simple and efficient gate-level modification to significantly reduce the area and power consumption. The main idea is to replace one of the RCA circuit with a Binary to Excess-1 Converter (BEC). The RCA module which propagates carry 1 is replaced by a BEC. The carry of RCA with carry 0 is passed through a BEC which is equivalent to the RCA with carry 1 and in turn reduces the area and power consumption

II. PROPOSED SYSTEM

The system is designed for two main purposes. First purpose is by adding a brent kung adder and BEC 1 into the carry select adder can reduce the power consumed and area required for the adder. And the other purpose is the triple fault tolerance in a carry select adder. To be fault tolerant, a system must have one or more redundant components that can take over the function when the primary component fails. In addition the system must have both a means of detecting failures in the component and a means of transferring to working components after a failure has been detected. Fault tolerant system configurations are used extensively in processes where the system must remain on line in the event of component failure.

A. Carry select adder

In electronics, a carry-select adder is a particular way to implement an adder, which is a logic element that computes the (n+1)bit sum of two n bit numbers. The carry-select adder is simple but rather fast, having a gate level depth of 0 √n. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry-in is known. The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs .When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays. Above is the basic building block of a carry-select adder, where the block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result

TABLE I TRUTH TABLE OF FULL ADDER ONE BIT

X	Y	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

B. Carry select adder with BEC

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. A regular CSLA circuit uses two RCAs through which the sum and carry outputs are generated. One of the RCA block propagates a carry „0" and the other RCA block propagates carry „1". Multiplexers are provided at each RCA block to select the carry output . This selection of carry outputs increases the speed of operation of the adder but require more area as it uses two RCAs and as a result it consumes more power. In order to reduce the area and power consumption a modified CSLA is proposed. The modified CSLA proposed in this project is a simple and efficient gate-level modification to significantly reduce the area and power consumption. The main idea is to replace one of the RCA circuit with a Binary to Excess-1 Converter (BEC). The RCA module which propagates carry „1" is replaced by a BEC. The carry of RCA with carry „0" is passed through a BEC which is equivalent to the RCA with carry „1" and in turn reduces the area and power consumption .It evaluates the performance of the proposed designs in terms of delay, area, power. Excess-3 binary coded decimal also called biased representation of Excess-N, is a

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complementary BCD cod and numeral system. It is a way to represent values with a balanced number of positive and negative numbers using a pre-specified number N as a biasing value. It is a non- weighted code. In XS-3, numbers are represented as decimal digits, and each digit is represented by four bits as the digit value plus 3 (the "excess" amount):
1. The smallest binary number represents the smallest value. (i.e. 0 − Excess Value).
2. The greatest binary number represents the largest value. (i.e. 2 N+1 − Excess Value − 1).
The primary advantage of XS-3 coding over non-biased coding is that a decimal number can be nines' complemented (for subtraction) as easily as a binary number can be ones' complemented (to invert all bits). As stated earlier the main idea of this work is to use BEC instead of the RCA with in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1 bit BEC is required.

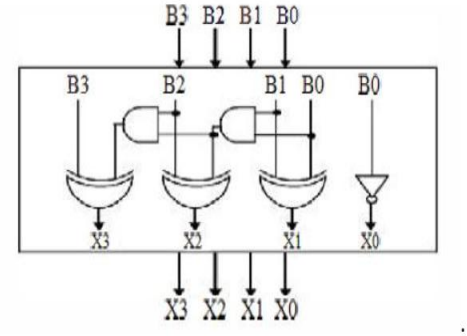

Fig.1 BEC

The Boolean expressions of 4-bit BEC are listed below, (Note: functional symbols, - NOT, & AND, /\ XOR).
XO = -BO
Xl = BO (l)/\Bl
X2 = B2 /\ (BO & Bl)
X3 = B3 /\ (BO & B 1 & B2)

C. Parallel Prefix Adders
Parallel prefix adders are used to speed up the binary additions as they are very flexible. The structure of Carry Look Ahead Adder (CLA) is used to obtain parallel prefix adders. Tree structures are used to increase the speed of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation.

The construction of parallel prefix adder involves three stages:
1. Pre- processing stage
2. Carry generation network
3. Post processing stage

❖ Pre-possessing stage - Generate and propagate signals to each pair of inputs A and B are computed in this stage. These signals are given by the following equations:
Pi=Ai xor Bi
Gi=Ai and Bi

❖ Carry generation network: In this stage, we compute carries equivalent to each bit. Implementation of these operations is carried out in parallel. After the computation of carries in parallel they are segmented into smaller pieces. Brent-Kung adder is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in Brent Kung adders. But the gate level depth of Brent-Kung adders is 0 (log2 (n)), so the speed is lower.

D. Fault-Tolerant
Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of (or one or more faults within) some of its components. If its operating quality decreases at all, the decrease is proportional to the severity of the failure, as compared to a naively designed system in which even a small failure can cause total breakdown. Fault tolerance is particularly sought after in high-availability or life-critical systems. The ability of maintaining functionality when portions of a system break down is referred to as graceful degradation.

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A fault-tolerant design enables a system to continue its intended operation, possibly at a reduced level, rather than failing completely, when some part of the system fails. The term is most commonly used to describe computer systems designed to continue more or less fully operational with, perhaps, a reduction in throughput or an increase in response time in the event of some partial failure. That is, the system as a whole is not stopped due to problems either in the hardware or the software. An example in another field is a motor vehicle designed so it will continue to be drivable if one of the tires is punctured. A structure is able to retain its integrity in the presence of damage due to causes such as fatigue, corrosion, manufacturing flaws, or impact.
Within the scope of an individual system, fault tolerance can be achieved by anticipating exceptional conditions and building the system to cope with them, and, in general, aiming for self-stabilization so that the system converges towards an error-free state. However, if the consequences of a system failure are catastrophic, or the cost of making it sufficiently reliable is very high, a better solution may be to use some form of duplication. In any case, if the consequence of a system failure is so catastrophic, the system must be able to use reversion to fall back to a safe mode. This is similar to roll-back recovery but can be a human action if humans are present in the loop.

III. RESULT

1. Designed a modified carry select adder.
2. Developed the program for an carry select adder and BEC
3. Identified the user friendly model of program for BK adder
4. Integrated the carry select adder with BEC and BK
5. Single fault tolerant model is developed

A. Designed a carry select adder
The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry-in is known.

❖ By using BEC
The basic idea of this work is to Binary to Excess-1 Converter (BEC) with cin=1 in the CSLA to achieve lower area and power consumption. The main advantage of this transistor level BEC-1 comes from the lesser number of MOS transistor than the Ordinary BEC-1.

❖ By using Brent kung adder
It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in brent kung adders. Brent-Kung adder is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs. The area of the adder designs is measured in terms of look up tables (LUT) and input output blocks (IOB) taken for Xilinx virtex 5 FPGA is plotted . ISE software doesn't give exact delay of the adders because it is not able to analyse the critical path over the adder

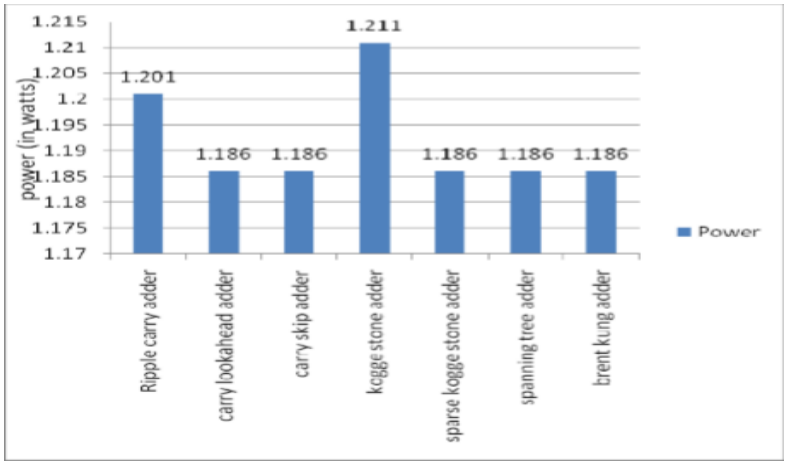

Fig. 5 Power observed in Xilinx

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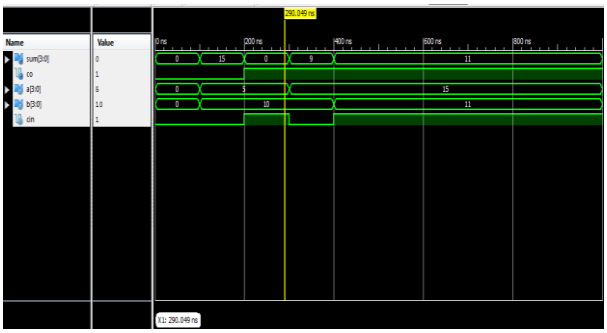
B. SIMULATION



c. Simulation Of Fault Tolerant Model

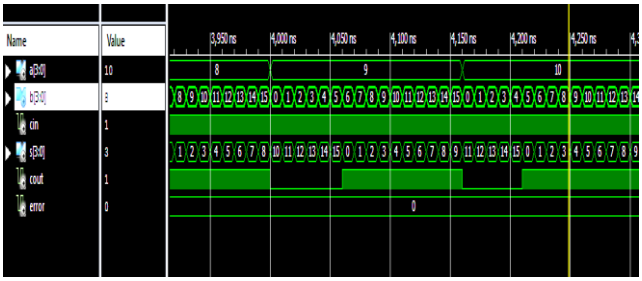


TABLE III COMPARISON

TYPE	POWER (Mw)	NUMBER OF SLICES(ns)	DELAY (area)
Regular CSLA	134	46	14.256
CSLA with BEC	133	31	12.188
Efficient CSLA	131	11	11.974

d. Advantages

- ❖ Less area (less complexity)
- ❖ Less power consumption
- ❖ More speed compared to regular CSLA

IV. FUTURE WORKS

1. Identify the double and triple fault tolerant architecture
2. Need to develop program for double and triple fault tolerant architecture
3. Implementation of triple fault tolerant architecture in modified carry select adder

The proposed system can be further extended for 16 bit, 32 bit, 64 bit word size. New architectures can be designed to reduce areas power and delay of the circuits. Steps may be taken to optimize other parameters such as frequency, clock cycle etc.

V. CONCLUSION

In the proposed work, a Modified Carry Select Adder is proposed which is designed using single Brent kung adder and Binary to Excess-l Converter instead of using single Ripple Carry Adder for Cin=0 and Ripple Carry Adder for Cin=l in order to reduce the delay and area consumption of the circuit. Here, the adder architectures are designed for 4-Bit word size only. This work can be extended for higher number of bits also. By using parallel prefix adder, delay and area consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore Brent Kung adder is used.

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The system presents fault tolerant adder design assuming single double and triple fault models. Our approach is area and power efficient compared to the traditional TMR approach. A triple fault tolerant architecture for modified carry select adder is designed. Generally more than one module near the error affecting part of the system becomes faulty. Hence the system must have the capability to tolerate multiple faults. And also it considers triple fault cases and show how a system can reconfigure from an error causing two faults at maximum

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